MULTI-PACKAGE STACK MODULE

CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims priority from Korean Patent Application No. 2002-65210 filed October 24, 2002, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electronic module, and more particularly, to a multi-package stack module made by stacking a plurality of semiconductor packages.

2. Description of the Related Art

The electronic industry continues to seek products that are lighter, faster, smaller, multi-functional, more reliable and more cost-effective. In order to meet the requirement of the electronic industries, circuit chips must become highly integrated.

However, it is expensive and there are technical limitations to enhancing the density of integration of chips. Therefore, 3-D type semiconductor packaging technologies have been developed and used in order to overcome the above-mentioned problems. In general, a multi-package module made by stacking a plurality of packages in a module is known.

In order to manufacture a multi-package module by using conventional ball grid array type packages, additional electrical connecting means need to be inserted between packages, because the conductive bumps are formed entirely on the rear side of each board and can induce structural mismatch with the chip of the package beneath.

Therefore, the packages in which bump pads are formed in the area peripheral to the chip installation area are usually used for manufacturing multi-package modules as shown in FIG. 1 and FIG. 2.

FIG. 1 is a plan view of a conventional package used in a multi-package module. FIG. 2 is a sectional view of a conventional multi-package module made by stacking a plurality of the conventional packages shown in FIG. 1. The conventional package of FIGS. 1 and 2 comprises a board (140), a chip (112) disposed on the board, a plurality of redistribution patterns (143) formed on the board, a plurality of first bump pads (144) and a plurality of second bump pads (145). The first bump pad (144) is electrically connected to one end of each redistribution pattern (143). The other end of the redistribution patterns (143) is electrically connected to the chip (112). The second bump pads (145) are formed on the rear side of the board (140) and are electrically connected to the first bump pads (144) through via-holes (146). In general, a plurality of bonding pads (114) are formed on the chip (112), and the bonding pads (114) are electrically connected to the redistribution patterns (143) by bonding wires (116). The chip (112) and the bonding wires (116) are usually encapsulated by a resin (160), such as epoxy molding compound (EMC), in order to protect the chip 112 from the adverse effects of the external environment. Solder bumps (170) are usually formed on the second bump pads (145). The solder bumps (170) are used for electrical connection between respective packages.

A plurality of the packages are stacked to form a multi-package stack module (100) as shown in FIG. 2. The stacked packages are electrically connected to each other by the solder bumps (170).

In the conventional multi-package module (100), the chips (112) which are placed in the stacked packages (100) are vertically aligned one with the other. This configuration is employed because the chip installation areas of the stacked packages are all identical. Therefore, each chip (112) is affected not only by the heat it generates, but is also affected by the heat generated by the upper and lower adjacent chips. In addition, the bump pads (144,145) and the solder bumps (170) must be formed in the area peripheral to the chip installation area. Therefore, the area in which the Input/Output terminals can be formed is limited.

SUMMARY OF THE INVENTION

Accordingly, the present invention has been conceived to solve the above- described problems.

In one embodiment, a multi-package module according to the present invention comprises a plurality of stacked packages. Each of the stacked packages comprises a board, at least one chip, a plurality of redistribution patterns, a plurality of first bump pads, a plurality of second bump pads and via holes. The board may be composed of a chip installation area and a bump pad area. The chip may be disposed in the chip installation area, and the first bump pads may be formed in the bump pad area. The first bump pads are electrically connected to the chip through the redistribution patterns formed on the board. The second bump pads may be formed on the rear side of the board, and preferably on the rear side of the chip installation area. The second bump pads are electrically connected to the redistribution patterns. In the multi chip module made by stacking a plurality of the above-described packages, each of the packages is electrically connected to the adjacent packages through electrical connectors such as solder bumps disposed between the second bump pads of the upper package and the first bump pads of the lower package. The chip installation areas of the adjacent packages are not in vertical alignment with each other.

Preferably, each package may comprise an encapsulation part protecting the chip from the external environment. More preferably, the height of the solder bumps may be similar to the heights of the encapsulation parts.

Preferably, the second bump pads may be formed on the entire rear side of the board of the lowest stacked package.

Preferably, at least one electronic device may be disposed on the board of the highest stacked package, and electrically connected to the second bump pads of the highest stacked package.

According to another embodiment, a multi-package module comprises a plurality of stacked packages including an upper package and a lower package. Each package has a board having located on a first side thereof a chip installation area and a bump pad area. At least one chip is disposed in the chip installation area chip. A plurality of first bump pads are formed in the bump pad area electrically connected to chip. The respective packages are electrically connected by connecting bump pads of the upper package to bump pads of the lower package. The chip installation area of the upper and lower packages are laterally offset from each other.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and the other aspects and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings, in which:

FIG. 1 is a plan view of the conventional ball grid array package used for manufacturing a multi-package module;

FIG. 2 is a sectional view of the conventional multi-package module made by using the packages described in FIG. 1;

FIG. 3 is a plan view of the ball grid array package used for manufacturing a multi-package module according to an aspect of the present invention;

FIG. 4 is a sectional view of the multi-package module according to a first embodiment of the present invention;

FIG. 5 is a sectional view of the multi-package module according to a second embodiment of the present invention; and

FIG. 6 is a sectional view of the multi-package module according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention will be described referring to FIG. 3 through FIG. 6. The structure of the package used for the multi-package module of the present invention will be described referring to FIG. 3 and FIG. 4. As shown in FIG. 3 and FIG. 4, a chip (212) is disposed on a side portion of a board (240) rather than a center portion of the board (240). The portion of the board (240) on which the chip (212) is disposed is hereinafter referred to as a chip installation area (241). The chip (212) may be attached to the chip installation area (241) by adhesives such as an epoxy. First bump pads (244) are formed on the remaining portion of the board (240) which is located outside the chip installation area (241). The portion of the board (240) wherein the first bump pads (244) are formed is hereinafter referred to as a bump pad area (242). Because the chip (212) is disposed on a side portion of the boards (240), the first bump pads (244) need not be located on the peripheral portion of the board (240). More specifically, the bump pad area (242) can occupy up to the full extent of the remaining portion of the board (240). In FIG. 3, the chip installation area (241) is positioned on about one half of a first side of the board (240), and the bump pad area (242) is positioned on about the other half of the first side of the board (240).

The first bump pads (244) are electrically connected to the redistribution patterns (243). Second bump pads (245) are formed on the second side of the board (240), and are electrically connected to the redistribution patterns (243) through via holes (246). Specifically, as shown in FIG. 4, the second bump pads (245) are formed on the second side of the boards (240) in the space corresponding to the chip installation area (241). A conductive bump such as a solder bump (270) is formed on each second bump pad (245).

Generally, bonding pads (214) are formed on the chip (212), and are electrically connected to the redistribution patterns (243) by electrical connectors such as bonding wires (216). The chip (212) and the bonding wires (216) are generally encapsulated by a member formed of a resin (260), such as EMC, in order to be protected from the adverse effects of the external environment.

A multi-package module (200) according to a first embodiment of the present invention will be described referring to FIG. 4. As shown in FIG. 4, packages such as those described in the FIG. 3 are stacked in a manner such that chips (212) of the stacked packages are not in vertical alignment with each other. In other words, the chips (212) of the stacked packages are laterally offset from each other. Preferably, the chips (212) do not overlap with each other. The solder bumps (270) of the upper package are electrically connected to the first bump pads (244) formed on the bump pad area (242) of the lower adjacent package. Because the solder bumps (270) are formed on the second side of the board (240) in a space corresponding to the chip installation area (241), the chip installation area (241) of the upper package becomes positioned above the bump pad area (242) of the lower packages. Therefore, the chip installation area (241) of the two adjacent stacked packages are not in vertical alignment with each other. Preferably, the second bump pads (245) and the solder bumps (270) are formed on the second side of the board (240) of the lowest stacked package.

FIG. 5 is a sectional view of a multi-package module (300) according to a second embodiment of the present invention. The basic structure of the multi-package module (300) is the same as that of the multi-package module (200) except for an additional electronic device (380) disposed on the bump pad area (342) of the highest package of the multi-package module (300).

The electronic device (380) may be a capacitor, an inductor, a resistor, or other electronic elements. Although one electronic device (380) is described in FIG. 5, a plurality of electronic devices can be disposed on the bump pad area (342). Preferably, the electronic device (380) is electrically connected to the first bump pad (344).

FIG. 6 is a sectional view of a multi-package module (400) according to a third embodiment of the present invention. The basic structure of the multi-package module (400) is the same as that of the multi-package module (200) except that at least one package is a multi-chip package. As shown in FIG. 6, at least two chips (412, 422) are stacked in a package and the two chips (412, 422) are electrically connected to redistribution patterns (443) by bonding wires (416, 426) and to bump pads (444, 445) by redistribution patterns (443). The number of chips employed can be determined according to their usage.

The multi-package module structure described in the specification can also be adapted to the system-in module including a memory, central processing units (CPUs), and other electronic devices in a single module.

Because of the configuration of the multi-package module described in the embodiments of FIGS. 3-6, it is possible to prevent chips in one location in a stacked package from being affected by the heat generated by chips of another adjacent stacked packages. In addition, it is possible to enhance the freedom of designing input/output terminals, because the bump pads need not be formed in the area peripheral to the chip installation area.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.